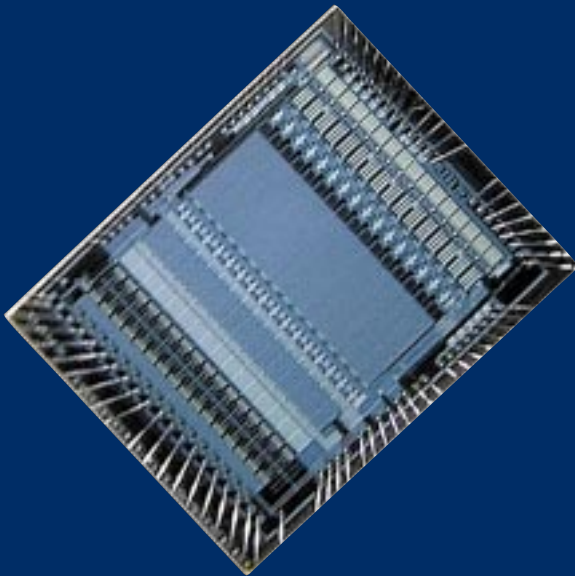


ACE™

Charge Readout Chip



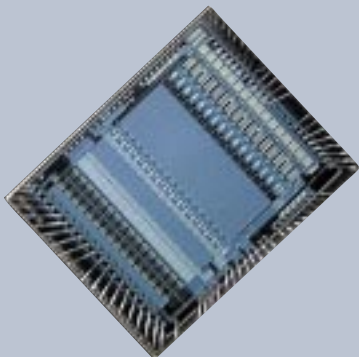
Advanced Charge-conversion Electronics

A multi-channel charge sensitive amplifier/shaper ASIC for reading position sensitive detector arrays

Standard Features	Applications
<p>16 Channels Signal Trigger Output Low Noise Large Dynamic Range Ultra High Linearity On-Chip 12-Bit Ultra-linear ADC Test Input</p>	<p>For applications that require high spatial and energy resolution position sensitive detector arrays from gamma-ray astronomy, nuclear physics to medical and industrial imaging. The ACE™ chip can be used with:</p> <ul style="list-style-type: none">• Multianode PMTs• PMTs and Avalanche Photodiodes• Silicon strip and pad detectors• Channeltrons & Microchannel Plates
Availability	Contact
<p>ACE™ is available as individual chips or integrated with position sensitive solid state detectors such as multianode PMTs, photodiode and avalanche photodiode (APD) arrays, silicon, GaAs, CdZnTe strip, pixel or pad detectors. Interface electronics with data acquisition software and test and evaluation systems can also be supplied.</p>	<p>NOVA R&D Inc. 1525 Third Street, Suite C Riverside, CA 92507-3429 Tel: (909) 781-7332 Fax: (909) 781-0178 nova@novarad.com www.pe.net/~nova</p>



ACE™ Specifications



Number of channels:	16
Power consumption:	208 mW per chip (13 mW/channel)
Full scale signal:	31 pC (700 MeV Si)
Dynamic range (full scale:threshold):	1400:1 (not self-triggering over the whole range) ~ 500:1 (self-triggering range)
RMS noise:	~ 100 keV
Gain variation:	≤ 10% *
Threshold variation:	≈ 10% rms at 3 MeV
ADC type:	12-bit high-linearity Wilkinson
Dead time per event:	≈ (6 + 0.125 N) μsec **
Integral nonlinearity:	≈ 0.1% of full scale
Max. leakage current cancellation:	1 μA
Chip size:	6.1 x 7.3 mm, 84 pads
Temperature coefficient of gain:	< ±20 ppm/°C
Offset temp. variation (-20°C to 40°C):	< 1 channel (after correction)
Cross talk for full scale pulse:	2 channels

* Among channels on one chip. Chip-to-chip variations can be larger.

** N = pulse height channel number, including pedestal.

Dead time could be reduced with higher ADC clock frequency.

The example shown assumes 8 MHz ADC clock.



R&D, Inc.