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Test Results of the Readout Electronics for Nuclear Applications (RENA) Chip Developed for Position-Sensitive Solid State Detectors

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Test Results of the Readout Electronics for Nuclear Applications (RENA) Chip Developed for Position-Sensitive Solid State Detectors

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Abstract

A mixed signal Application Specific Integrated Circuit (ASIC) chip for front end readout electronics of position sensitive solid state detectors has been developed. It is called RENA (Readout Electronics for Nuclear Applications). This chip can be used for large number of channels and high energy resolution astrophysics and nuclear physics detectors. It can also be used for medical and industrial imaging of x-rays and gamma rays. The RENA chip is a monolithic integrated circuit and has 32 channels with low noise charge sensitive amplifiers followed by a polarity amplifier and a high quality shaper circuit. It works in pulse counting mode with good energy resolution. It also has a self triggering output which is essential for nuclear applications when the incident radiation arrives at random. Different, externally selectable, operational modes that include a sparse readout mode are available to increase data throughput. It also has externally selectable shaping (peaking) times. A full scale prototype RENA chip has been manufactured. The preliminary results of tests done on the prototype chip are presented.

Keywords: Electronics, ASIC, Mixed signal ASIC, Front-end electronics, CdZnTe detectors.

1. RENA Chip Design

The RENA chip was developed as a low noise general purpose monolithic application specific integrated circuit (ASIC) front end readout electronics chip for most types of sensors, transducers or detectors that produce a charge pulse output and have many channels. For example, it can be used with all types of solid state radiation detectors such as silicon strip, silicon pixel, silicon drift, silicon PIN photodiode, germanium, CdZnTe, CdTe, HgI₂, and GaAs. It was designed with a self trigger output so that random signals without an external trigger can be processed. It has several different externally selectable integration (peaking) times to accommodate different charge collection times for different detectors. It also has several readout and data acquisition modes for versatile implementation and for detailed diagnostic testing. Great effort was spent to make this chip low noise and practical. For example, it has no external adjustments other than the functional settings for user friendly instrument development.

1.1 RENA Chip Circuit Design¹

A low noise charge sensitive amplifier with a capacitive integrator is used at the input (Figure 1). The input gate of the amplifier was optimized for 6 pF detector capacitance. However, new versions can be fabricated optimized for other input capacitance requirements. The input amplifier is designed to have a large open loop gain. The large open loop gain is expected to reduce noise and improve response to high capacitance detectors.

The input of the RENA chip can be programmed externally to accept positive or negative charge. A switch is placed in front of the polarity buffer (Figure 1) to connect the charge sensitive amplifier output to either the negative or the positive input. This allows for a symmetrical system so that the RENA chip will have a nearly identical response to both the negative and positive input signals.

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One shaper circuit is used in the RENA chip. The shaper circuit (Figure 1) have circuitry to produce a linear response with selectable peaking times. The shaper produces a clean unipolar pulse. Its peak is accurately proportional to the magnitude of the input charge. Eight peaking times are externally selectable with values from 400 ns to 6 μ s. The output of the second shaper is sent to an accurate peakhold circuit. Two comparators are connected to the output of the peakhold circuit, one for producing a low threshold trigger output and the other for high threshold discrimination. If interesting events are in a narrow energy band the two comparators can be set to enclose this band, therefore reducing noise and data throughput requirements. The comparators are leading edge type. The low threshold comparator output from each channel are ORed together to produce a single self trigger output to the external data acquisition system that signals the arrival of a legitimate event (Figures 2 and 3). The output of the high threshold comparator is only provided as an output for external use such as large pulse event rejection or for accepting events that occur inside an energy window.

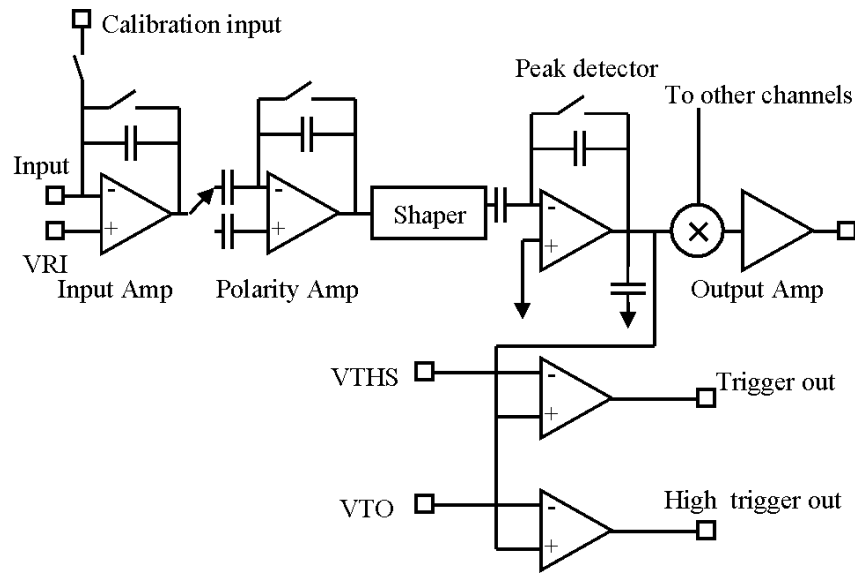


Figure 1. Block Diagram of the analog section of the RENA chip.

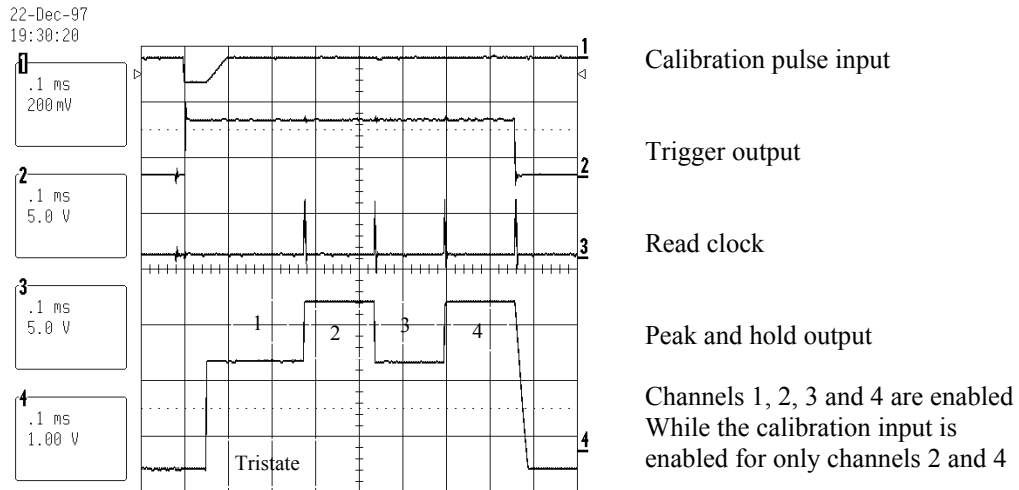


Figure 2. Typical input and output signals of a prototype RENA chip where the top signal is the Calibration pulse in, second one is the self trigger out, third is the read clock in and the bottom signal is the analog output where the four channels are turned on but only the second and the fourth channel's calibration inputs are enabled.

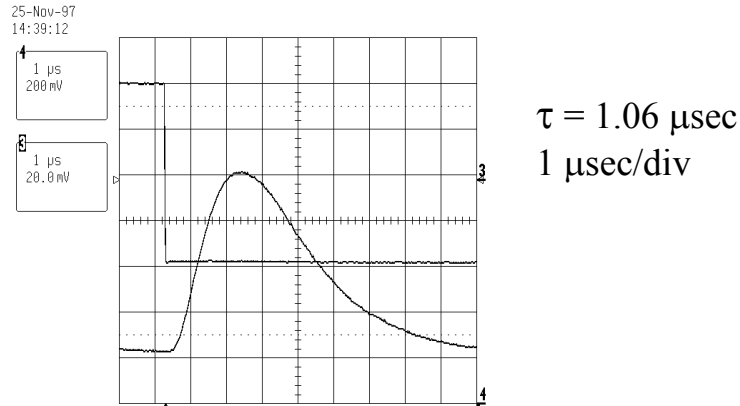


Figure 3. The bottom signal is the shaped signal output of the calibration input pulse and the top signal is the calibration input pulse.

The output of the peakhold circuit is buffered and connected to the chip output through an analog multiplexer. Only one channel is connected to the output at a time. Each readout sequence consists of the peak and hold analog output, 4 bit chip address and 5 bit channel address. There is internal digital logic which allows automatic readout of the channels that have data (low threshold comparator triggered) called the sparse readout mode [1].

1.2. RENA Chip Specifications

The RENA chip is a charge sensitive 32 channel mixed signal ASIC chip (Table I). The present version has a dynamic range of 50,000 electrons and maximum output swing of 2 volts. The input is single ended with the input amplifier referenced to an external low noise reference voltage. Each of the 32 channels' peak and hold outputs are multiplexed to a single analog output buffer. The specifications of the RENA chip are shown in Table I.

Table I. RENA chip specifications.

Number of channels	32 + two test channels
Trigger modes	Global trigger: All enabled channels read upon when any channel is triggered Sparse readout: Only the channels that have been triggered are read out Neighbor readout: Adjacent channels also readout in addition to sparse readout External delay trigger: Delay the disabling of non-triggered channels (see text) Select all: Read enabled channels on an external trigger pulse
Trigger threshold	Voltage input, 1.5 V to 3.5 V
Readout data	Channel and chip addresses, pulse height and high threshold set bit
Analog output settling time	≈ 500 ns per channel
Daisy chain	Up to 16 chips can be daisy chained to be readout as a single chip
Power	340 mW per chip
Test output modes	Enable any one channel for continuous output of the peakhold or shaper output
Peaking time	0.4, 0.73, 1.06, 1.34, 1.73, 3.17, 4.61 or 6.05 μs
Dynamic range	≈ 1 ke to 50 ke FWHM input for 1.5 to 3.5 V output (4.5 to 225 keV for CdZnTe)
Input referred noise	≈ 180 e rms @ 0 pF with 8 e rms/pF slope
Die size	4.932 x 6.906 mm

1.3. RENA Chip Readout Modes

The RENA chip has several different readout modes (Table I). In the SPARSE mode only channels that are enabled and triggered (have a signal above the threshold of the low level comparator) are read out. In the GLOBAL mode all channels that are enabled are read out when a trigger occurs. The SELECT ALL mode allows an external trigger to initiate readout of

all enabled channels. Normally once a channel is triggered the rest of the channels get disabled within 2 to 40 ns. In the EXTERNAL DELAY TRIGGER mode the disabling of the other channels, after a trigger, can be delayed by an external signal. In the NEIGHBOR mode the nearest (adjacent) channels immediately above and below the channel that was triggered are also readout. This mode is important if charge sharing between detector channels is expected to happen with significant probability in strip detectors.

1.4. Daisy Chaining RENA Chips

Up to sixteen RENA chips can be daisy chained together. When they are daisy chained they can be read out as if they are a single chip with more channels. This is required for detectors which have more channels than the ASIC chip, such as strip detectors. For example, a CdZnTe strip detector with 128 strips on each side can be readout by four RENA chips daisy chained together on each side. This arrangement will look like one chip to the readout electronics and the data acquisition and analysis program.

1.5. RENA Chip Input/Output

Figure 2 shows a typical oscilloscope screen dump of several input and output waveforms for a single readout sequence. In this figure four channels were enabled in which only the second and fourth channels were enabled for test pulse input which is clearly seen in the figure (bottom trace). The readout mode is the GLOBAL mode so that if any enabled channel gets triggered all enabled channels will be readout. Figure 2 also shows the calibration pulse input (top trace), the self trigger output (second trace), the read clock input (third trace). Figure 3 shows the shaped signal output from a real detector (two-dimensional CdZnTe pad detector) attached at its input, (bottom trace) and the trigger output for this signal (Top trace). The shaping time was set for 1.06 μ s.

2. Tests Carried Out on RENA Chip Using a CdZnTe Pad Detector Array

2.1. RENA Chip Mounting

Figure 4 shows a RENA chip mounted on a ceramic carrier. A dime is used to show the size. The output pad pitch is fanned out to 0.5 mm to accommodate PCB mounting and easy connection to external detectors with ultrasonic wire bonding. The ceramic carriers were designed to abut with each other so that a long chain of detectors can be made. If the silicon strip or other detectors have a pitch between about 0.25 and 0.5 mm, then the chip can be directly mounted onto the PCB next to the detector strips or pads. This will allow direct bonding of the input pads to the detector strips.

2.2 CdZnTe Two Dimensional Pad Array

Figure 5 shows the CdZnTe two-dimensional pad array used in testing the RENA chip. There are 32 pads (4 x 8) with a 3 mm pitch. One RENA chip can read all the 32 pads at the same time. The pads are not seen in the photograph as they are underneath facing the ceramic detector carrier. The detector is \approx 2 mm thick and made from two separate square sections to increase yield. The bias voltage is supplied to the top of the detectors.

2.3. RENA Chip and CdZnTe Pad Array Test Results

Preliminary tests of the RENA chip have been performed which included its functionality and noise characteristics. The preliminary noise measurement with respect to input capacitance is shown in Figure 6. It shows \approx 180 e⁻ rms noise @ 0 pF input with 8 e⁻ rms/pF slope. This measurement is performed by placing a capacitance directly into one of the inputs of the RENA chip as shown in Figure 6. This arrangement references the capacitance to the reference voltage (V_{RI}) on the PCB board.

A second measurement was performed where the capacitance is referenced to the reference voltage (V_{RI}) on the chip. This measurement and the connection diagram of the capacitors are shown in Figure 7. This arrangement produces lower noise which can be seen from the measurement with about 6 e⁻ rms/pF slope. This could indicate that there may be a slight difference in the V_{RI} on the chip and on the PC board.

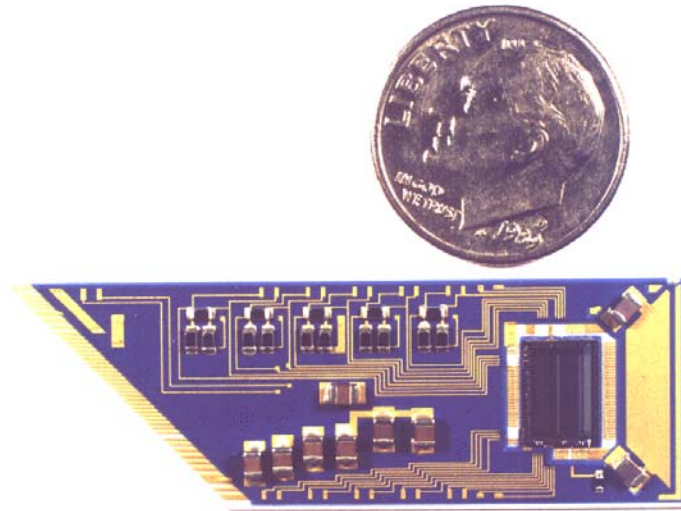


Figure 4. A RENA chip mounted on a ceramic carrier designed to accept detector outputs with ≥ 0.5 mm pitch.

a)



b)

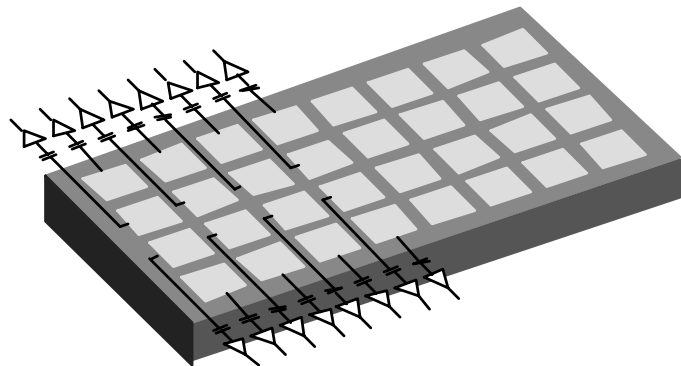


Figure 5. The CdZnTe pad detector used for testing the RENA chip. a) A photograph of the position sensitive CdZnTe pad detector with 32 (4 × 8) pads. A schematic concept drawing for CdZnTe pad detector also showing how the input of the RENA chip is connected to the pads.

Measurements on the gain linearity over the entire operating range of the RENA chip have been performed. The measurements were performed by supplying a pulse to the test input of the chip and measuring the voltage output. The results are shown in Figure 8 and indicate that the linearity of the gain is about a factor of two better than the design specifications.

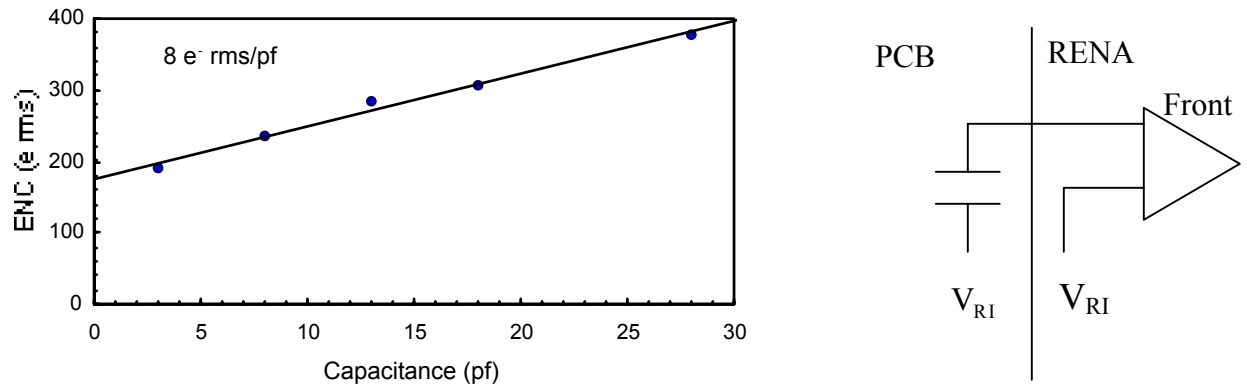


Figure 6. Noise vs. input capacitance measurement made through the Peak/Hold circuit with the capacitor directly connected to the RENA chip input reference voltage

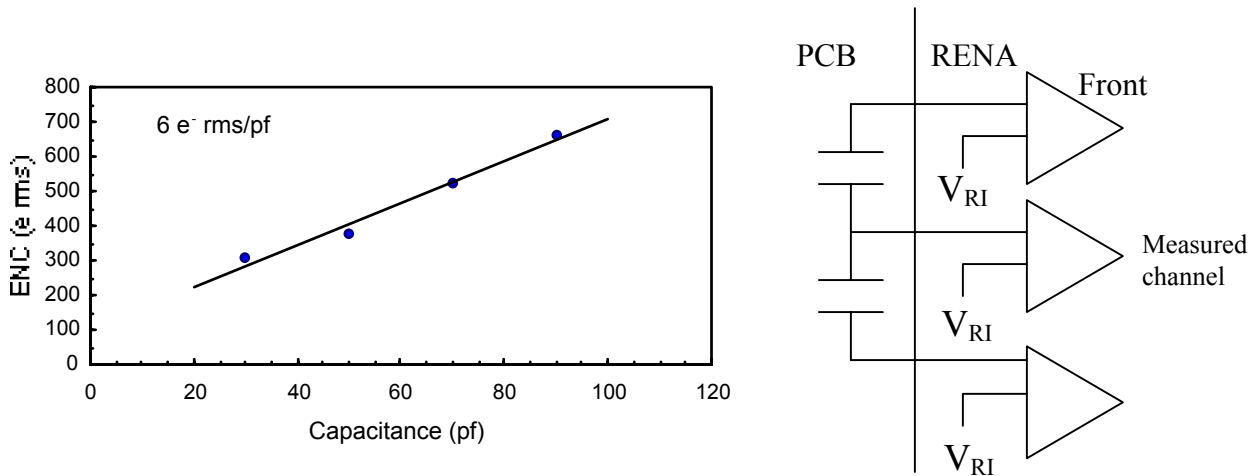


Figure 7. Noise vs. input capacitance measurement made through the Peak / Hold circuit with capacitors connected to adjacent channel inputs.

The CdZnTe detector shown above (Figure 5) was used in conjunction with the RENA chip to obtain x-ray spectra of ^{241}Am , one of which is shown in Figure 9. The 59.5 keV peak has a width of about 3.36 keV FWHM calculated using the untrapped side of the spectrum. This is the first spectra we have seen obtained from a CdZnTe detector using a multi channel mixed signal ASIC chip with self trigger output. The full chip is used with peak/hold output and sparse readout mode. The measurement was done at 85 °F, above room temperature. The spectrum was obtained by a conventional 16 bit ADC with the three lowest bits dropped to improve the differential non-linearity. It may be better to use a Wilkinson type ADC with high differential linearity to improve this spectra further.

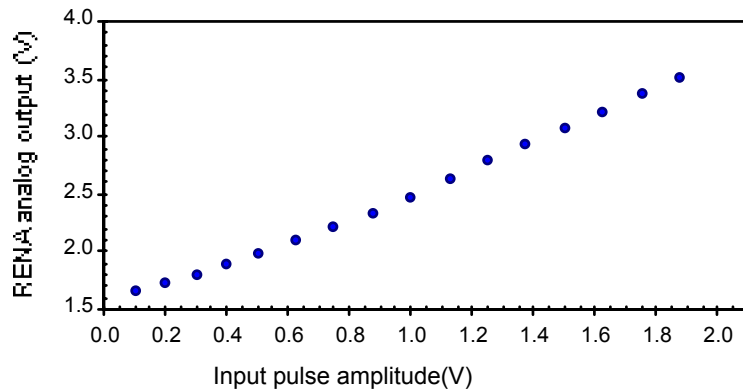


Figure 8. The RENA chip linearity measurement. Output voltage v.s. input test pulse voltage is plotted. Design specifications for the linearity at lower 1/4 of the curve was 10% and for the upper 3/4 of the curve was 5%. The measured linearity curve is significantly better by about a factor of 2.

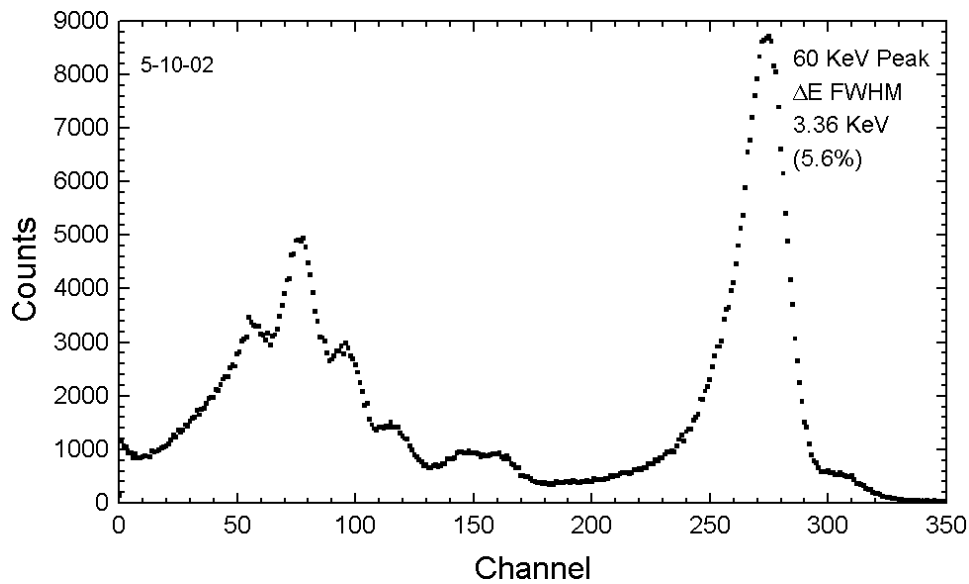


Figure 9. A spectrum of ^{241}Am obtained with the CdZnTe pad detector mounted to a prototype RENA chip. Peak and hold output digitized by a conventional 13 bit ADC (85 °F) (full chip).

Further tests were made only on the analog section of the RENA chip to understand its low noise capability by putting the chip into continuous output follower mode where the peak/hold is disabled and the shaped output signal of the selected channel appears at the output of the chip. This output is then amplified and put into a Tennelec pulse height analyzer. The resultant spectrum is given in Figure 10 which was taken at 45 °F. It shows significant improvement in noise and the spectrum has markedly better energy resolution, 2.72 keV FWHM. Spectrum at slightly lower temperature is shown here to show the capability of the chip.

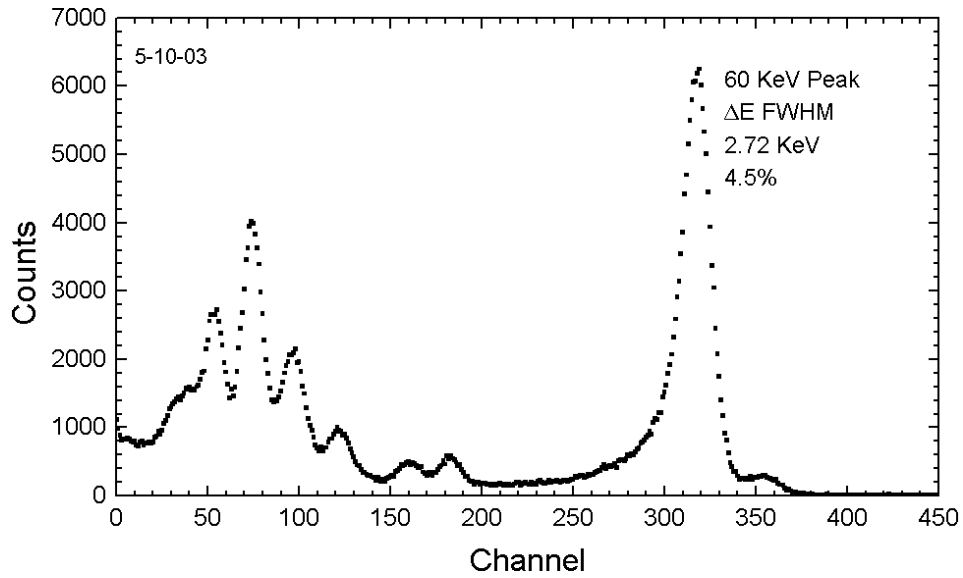


Figure 10. A spectrum of ^{241}Am obtained with the CdZnTe pad detector mounted on to a prototype RENA chip. The peakhold output is not used. The spectrum is obtained using the follower mode on RENA and the shaped output is analyzed using an external pulse height analyzer. Shaper output sent to PHA (45 °F) (analog section only).

A spectra at higher energies is shown in Figure 11 using ^{57}Co spectrum. The 122 keV peak is excellent for CdZnTe detectors with 5.76 keV energy resolution. The 14 keV low energy line is very sharp and clear. The noise level in all the spectra is low. Therefore, the CdZnTe pad detector's low energy threshold using the RENA chip is about a few keV.

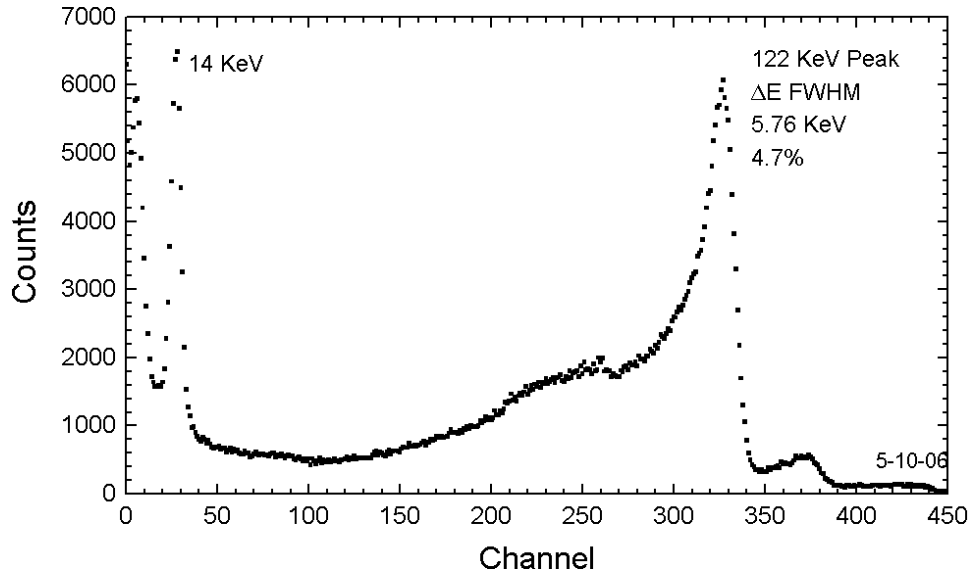


Figure 11. A spectrum of ^{57}Co obtained with the CdZnTe pad detector mounted on to a prototype RENA chip. The peakhold output is not used. The spectrum is obtained using the follower mode on RENA and the shaped output is analyzed using an external pulse height analyzer. Shaper output sent to PHA (48 °F) (analog section only).

3. Conclusion

An ultra low noise versatile mixed signal front-end electronics ASIC chip for solid state detectors and other charge output devices have been developed. The present chip is optimized for 6 pF detector capacitance. Other versions are planned to be fabricated and optimized for lower or higher detector capacitance. In the future we plan to include an on-board, high accuracy ADC for full digital output. Custom modification and optimization for specific applications is also straightforward. Radiation hard versions can be fabricated for applications in high radiation environments.

4. Acknowledgments

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5. References

1. C. Haber, et al., IEEE Trans. on Nucl. Science, **37**, No. 3, p. 1120, (1990).