NOVA R & D Inc.
1525 Third St., Suite C
Riverside, CA 92507, USA
www.novarad.com

Tel: 909.781.7332
Fax: 909.781.0178
nova@novarad.com

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NOVA R&D, Inc., 1525 Third Street, Suite C, Riverside, CA 92507, U.S.A.
U.S. Army ARDEC, Picatinny Arsenal, NJ 07806, U.S.A.
Innovative Design, 33501 Nancy Jane Ct., Dana Point, CA 92629, U.S.A.

Front-End Electronics for Spectroscopy Applications (FESA) IC[1]

M. Clajus[2], T. O. Tümer[2], G. J. Visser[2], S. Yin[2], P. D. Willson[3], and D. G. Maeding[4]
[2]NOVA R&D, Inc., 1525 Third Street, Suite C, Riverside, CA 92507, U.S.A.
[3]U.S. Army ARDEC, Picatinny Arsenal, NJ 07806, U.S.A.
[4]Innovative Design, 33501 Nancy Jane Ct., Dana Point, CA 92629, U.S.A.

Abstract

Non-destructive evaluation and inspection using x-rays require the detection of large photon fluxes. Typically, this requirement is met by operating the detectors in current mode, at the expense of the ability to measure the photon energy. This makes it necessary to obtain the energy information by other means, such as varying the energy of the x-ray source. We have developed an integrated circuit for the fast readout of solid-state x-ray and gamma ray detectors with multi-energy capability. The 32-channel Front-end Electronics for Spectroscopy Applications (FESA) chip is designed to handle photon rates in excess of one million photons per second per channel. In each channel, the detector pulses are shaped and amplified and then processed by a simple pulse-height analyzer that consists of five comparators each of which is connected to a dedicated counter. The 160 counters on each chip can be read out in less than 25 µs. The FESA IC features digitally controlled gains and offsets, a calibration input, and an analog test output, both of which can be connected to any channel. The five comparator threshold voltages, common to all channels, are provided externally, as is the current that controls the pulse shaping time.

I. INTRODUCTION

Non-destructive evaluation (NDE) and inspection (NDI) using x-rays require the detection of large photon fluxes with good spatial resolution, on the order of 1 mm or better. Typically, for lack of suitable integrated readout electronics that can process photon pulses at the required rates and provide the channel count needed, this is done by operating the detectors in current mode. In this mode, the charge generated by the photon interactions in the detector material is integrated without regard to individual photon pulses. As a consequence, pulse-height information that could be used to determine the photon energy spectrum is not available. On the other hand, that information is essential in cases where the chemical composition of the material under inspection needs to be determined, for example to identify contraband hidden in baggage or cargo [1], or for bone densitometry.. This determination requires the measurement of x-ray absorption by the material for at least two photon energy bands, from which an "effective" atomic number, Z, for the material along the ray path can then be obtained. Due to the lack of direct photon energy information mentioned above, this parameter has to be obtained indirectly, for which one of two methods is usually employed. In the first method, the x-ray source energy is varied periodically by modulating the tube voltage. Absorption data are taken near the maxima and minima of the modulation signal, effectively creating a dual-energy source. Apart from the technical effort required to perform the modulation, the energy information, in this case, is obtained at the expense of reducing the available data acquisition time per energy by more than a factor two. In the second method, the x-ray detection system consists of two stacked detector layers of suitable thicknesses. Low-energy photons are almost completely absorbed and detected in the first layers, leaving mostly high-energy gammas for the second layer. Again, the doubling of the number of channels that this requires represents a significant effort in order to achieve a very moderate energy resolution, given the broad spectrum of the x-ray sources used and the statistical nature of the absorption process.

In order to enable direct energy measurements for NDE and NDI purposes, we have developed a multi-channel mixed-signal ASIC for the fast readout of solid-state x-ray and gamma ray detectors with multi-energy capability. Each of the FESA (Front-end Electronics for Spectroscopy Applications) chip's 32 readout channels can process individual photon signals at rates up to one million counts per second and more. The design of this ASIC is described in Section II; its performance is discussed in Section III.

II. DESIGN OF THE FESA ASIC

The FESA chip has 32 detector readout channels. As shown in Figure 1, each channel consists of an inverting, charge-sensitive, continuous-reset amplifier, a second amplifier stage with individually programmable gains and offsets, and a coarse pulse height analyzer (PHA). This PHA, in turn, consists of five comparators and associated counters. Fast readout logic minimizes dead time by enabling the 160 counters on the chip to be read out in ≈ 20 µs. Two additional, analog-only channels, one at each end of the chip, are provided in order to avoid any problems that might result from

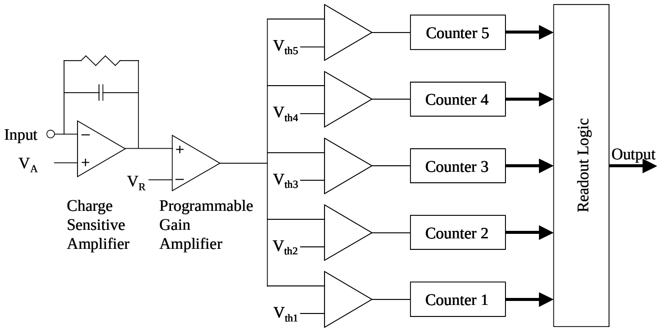

Figure 1. Block diagram of a single detector readout channel on the FESA chip.

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[1] Supported by U.S. Army ARDEC and the U.S. Department of Agriculture under Contract Number DAAA21-93-C-1014.

variations of performance parameters for the outermost channels. These “test” channels are identical to the analog part of the 32 full channels in every respect, but are not connected to any comparators or counters.

When a detector pulse reaches a readout channel, it charges the input capacitor with a time constant that is determined by the feedback capacitance and the input amplifier’s forward impedance. This time constant is fast compared to the typical charge collection times of solid-state detectors. The signal voltage is restored by a lower speed feedback impedance, which is realized as an active transconductor circuit. The value of this impedance, and therefore the signal decay time, is controlled by an external current, I_τ. Additionally, a second capacitor can be switched into the feedback circuit, parallel to the one shown in Figure 1, to provide a separate range of slower shaping times; the nominal ratio of the total capacitances in the two cases is 5.5:1. Both the control current and the switch for the second capacitor are common to all channels, so the shaping time will be uniform for the entire chip. The input amplifier is optimized for a detector capacitance of 2 pF.

The gain stage of each FESA channel consists of two operational amplifiers, each with individually programmable gains. This results in separate coarse (two bits) and fine controls (three bits) for the gain on each channel, which allow the user to vary the gain by up to a factor three to compensate for gain variations due to shaping time changes, process variations, and different detector output levels. An eight-bit DAC on each channel adjusts the baseline offsets, with a step size of approximately 16 mV. A “polarity” input can be used to globally shift the signal baseline up or down by 1.5 V, thus moving it closer to either rail and optimizing the available offset range for the signal polarity to be detected.

For test and calibration purposes, the chip provides a test signal input that can be capacitively coupled to any of the channels. The amplifier output signals that are sent to the comparators can be monitored on a test output pad; any one channel at a time can be connected to this pad.

The gain and offset controls as well as the bits selecting which channel(s) should be connected to the test inputs and outputs are loaded into the chip using a 34-bit serial shift register (one bit for every channel). Once the shift register is loaded, its values are strobed into one of fifteen latches per channel – one latch for each control function. The specific latch to be strobed is selected by four address lines.

The five threshold voltages for the comparators are provided externally, common to all channels. To avoid spurious counts due to noise superimposed on a signal close to a threshold, the comparators each have a voltage hysteresis. This solution has two drawbacks when trying to count signals with low amplitudes: the hysteresis limits how close the threshold can be set to the signal baseline, and it lowers the photon rates at which pulse pile-up starts to significantly affect the measured count rates. The latter problem occurs because the trailing edge of a signal pulse does not just have to drop below the threshold before the next pulse can trigger the comparator again, it has to undershoot the threshold by the amount of the hysteresis. To minimize these two drawbacks without sacrificing the noise tolerance that the hysteresis offers, the first two comparators on each channel, which are intended for detecting the low amplitude signals, have a smaller hysteresis, by a factor two, than the remaining three comparators. Different signal polarities are accommodated by a polarity input, which is separate from the one on the analog part of the chip and controls the sign of the hysteresis and whether the comparators trigger on the positive- or negative-going edges of the signals.

Each comparator output is connected to an 18-bit ripple counter via an AND gate, whose second input receives the count enable signal. When this signal is asserted, the comparator output pulses reach the counter inputs and are counted. When count enable is deasserted, the pulses are blocked, ensuring that the counter values remain unchanged, for example, during readout. All counters can be reset by asserting a count reset signal while count enable is low.

The counters are read out by asserting read enable and shifting a single signal (logic high) through a 160-bit shift register. Each bit corresponds to one counter, whose count value is sent to the eighteen data output lines – one for each counter bit – when the shift register bit is set. The period of the shift register clock can be as low as 120 ns; including a 161st bit that is used to turn off the data output buffers and the time required for setting up the read enable signal and resetting the counters, this leads to a total readout dead time of approximately 20 µs.

The readout shift register can also be used while the counters are enabled, to connect any selected counter to the data output buffers for monitoring purposes. The corresponding comparator output can be monitored at a separate pad at the same time. Also for test purposes, the comparator inputs for the entire chip can be connected to a test signal input instead of the individual amplifier outputs.

An enlarged photograph of the FESA ASIC, indicating some of the major functional blocks, is shown in Figure 2. The overall chip size is 7.3 × 10.0 mm^2.

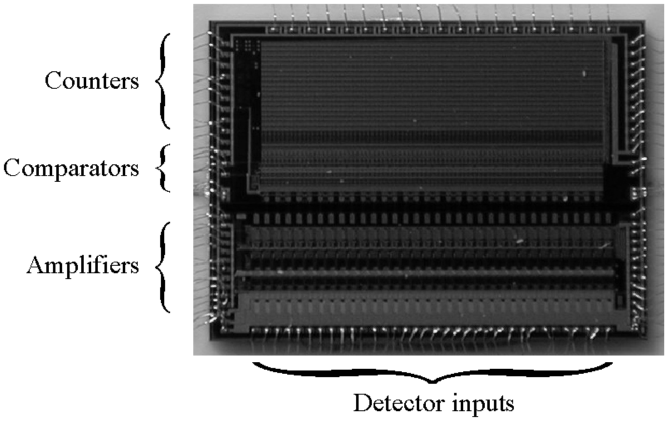

Figure 2. Photograph of the FESA chip, showing some of the main functional blocks.

III. PERFORMANCE OF THE FESA CHIP

Preliminary operation parameters and performance data of the FESA chip have been measured. These include, on the analog side of the chip, the dependence of the signal shaping times on the current I_τ, the calibration of the gain and offset DACs and the linearity of the latter, and signal noise levels. On the digital part of the chip, we checked for channel-to-channel variations of the actual comparator thresholds and hystereses, and measured the rate capabilities, both with regular (test pulser) signals and with random x-ray photons.

Signal decay times (90% to 10%) in the fast shaping time range were found to vary between about 60 ns and 280 ns as the control current was decreased from 60 µA to 10 µA. Figure 3 shows an examples of a typical pulse. In the slow range, the decay times vary between 350 ns and 1.6 µs.

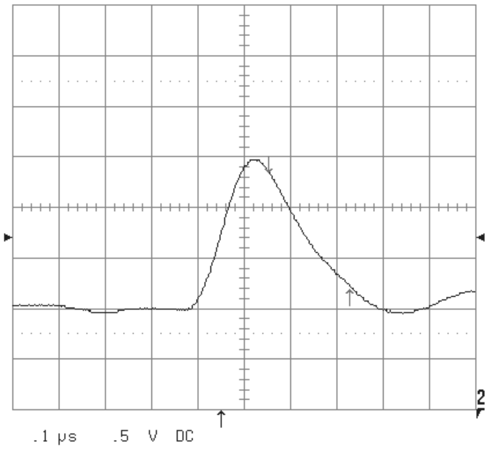

Figure 3. Typical output pulse from the amplifier section of the FESA chip..

The effect of the gain control bits was found to be in good agreement with design specifications and simulations. The two first-stage, coarse control bits vary the gain by slightly more than a factor two, in geometric steps. The three fine control bits provide a linear gain variation by approximately 40%. The offset DACs typically have slopes between 15 and 16 mV/count – compared to a design value of 16 mV/count – with average deviations from the linear fit on the order of 1 mV.

Preliminary measurements of noise levels at the analog monitor output indicate an input-referred rms value of about 1000 electrons, which for CdZnTe detectors would correspond to about 4.5 keV. While this is somewhat higher than the design goal of 3 keV, it is still very much compatible with most of our target applications, which emphasize rate capability more than excellent energy resolution, but require some basic energy information.

To measure thresholds, we sent rectangular pulses to the comparator test input and observed, for a given external threshold voltage, what amplitude it took to trigger the comparators. Similarly, by observing how far we had to lower the signal to reset a triggered comparator, we were able to measure the hysteresis. The thresholds generally reproduce the externally supplied values well, with a slight increase, ≈20 mV, from one end of the chip to the other. To verify that this was a real threshold variation rather than just a degradation of the test signal as it got distributed in the chip, we used the amplifier output signals. When no pulses are applied to the amplifier inputs and the offsets are adjusted to be just below or above the comparator thresholds, noise fluctuations can be enough to trigger a few counts. The offset range over which this happens exhibits the same variation across the chip as the thresholds measured using the comparator test input. Note that this phenomenon can be used to calibrate the offsets to match the threshold variation and thus cancel its effect in terms of photon energy thresholds. There is also a difference in trigger thresholds between the low- and high-hysteresis comparators, which is about equal to the hysteresis difference between the two comparator types; in effect, there is agreement between the lower (turn-off) thresholds. The hystereses themselves do not exhibit any significant dependence on channel number, but are typically a factor of two below the design values (25 and 50 mV instead of 50 and 100 mV).

The rate capability of the FESA chip was measured both by sending a train of rectangular voltage pulses from a pulse generator to the analog test input and by connecting a CdZnTe detector array to its detector inputs and irradiating it with high x-ray fluxes. In the former case of a regular signal, we were able to handle pulse rates up to 2.5 MHz. Note, however, that the FESA amplifiers produce two pulses for every input pulse, one on the rising edge and another, of opposite polarity, on the falling edge. The need to keep those two pulses separated limited the input signal frequency. Improved tests using a pulsed LED and a photodiode, which do not suffer from this limitation, are in preparation. In the x-ray measurements, the achievable rates depended strongly on the quality of the detector arrays used; for the best detectors, the rates reached between one million and 1.5 million counts per pixel per second before pile-up limited any further increases. This shows that the primary design goal in developing the FESA chip, a rate capability of at least one million counts per second per channel, has been reached.

IV. REFERENCES

[1] T. O. Tümer et al., “Preliminary Results Obtained from a Novel CdZnTe Pad Detector and Readout ASIC Developed for an Automatic Baggage Inspection System,” Presentation at this conference.