Readout Electronics for Nuclear Applications (RENA) Chip

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Abstract

A Readout Electronics for Nuclear Applications (RENA) Chip has been developed to read out position sensitive solid state detectors for the nuclear instruments. This chip can also be used for medical and industrial imaging of x-rays and gamma rays. It is a multi channel monolithic mixed signal application specific integrated circuit (ASIC) chip. The RENA chip has 32 channels with low noise charge sensitive amplifier inputs. It works in pulse counting mode with good energy resolution. It also has a self triggering output which is essential for nuclear applications when the incident radiation arrive at random. Different, externally selectable, operational modes that includes a sparse readout mode is available to increase data throughput. The design of the chip and the results of tests done on a full scale prototype chip will be presented.

I. RENA CHIP DESIGN

The RENA chip was developed as a very low noise general purpose monolithic Application Specific Integrated Circuit (ASIC) front end readout electronics chip for most types of sensors, transducers or detectors that produce charge as output. For example, it can be used with all types of solid state radiation detectors such as the silicon strip, silicon pixel, silicon drift, silicon PIN photodiode, germanium, CdZnTe, CdTe, HgI_2, GaAs, etc. It was designed with self trigger output so that random signals without an external trigger can be processed. It has several different externally settable integration (peaking) times to accommodate different charge collection times for different detectors. It also has several readout and data acquisition modes for versatile implementation and also for detailed testing. Great effort was spent to make this chip low noise and practical. For example, it has no external adjustments other than the functional settings for user friendly instrument development.

A. RENA Chip Circuit

A very high input impedance charge sensitive amplifier with a capacitive integrator is used at the input (Figure 1). The input gate of the amplifier is optimized for 6 pF input capacitance for this version. However, new versions can be fabricated optimized for other input capacitance requirements. The input amplifier is designed to have large open loop gain. The large open loop gain is expected to reduce noise and improve response to high capacitance detectors.

The input of the RENA chip can be programmed externally to accept positive or negative charge. A switch is placed in front of the polarity buffer (figure 1) to connect the charge sensitive amplifier output to either the negative or the positive input. This allows a symmetrical system so that the RENA chip will have nearly identical response to both the negative and positive input signals.

Two shaper circuits are used in RENA. Both shapers I and II have circuitry to produce a linear response with selectable peaking times (Figure 1). Combination of shapers I and II produce a bell shaped unipolar pulse. Its peak is accurately proportional to the magnitude of the input charge. Eight peaking times are externally selectable with values from 400 ns to 6 μs. The output of the second shaper is sent to an accurate peakhold circuit. Two comparators are connected to the output of the peakhold circuit, one for producing a low threshold trigger output and the other for high threshold discrimination. If interesting events are in a narrow energy band the two comparators can be set to enclose this band, therefore reducing noise and data throughput requirements. The comparators are leading edge type. The low threshold comparator output from each channel is sent to an OR circuit which produces a single self trigger output to the external data acquisition system that signals the arrival of a legitimate event. The output of the high threshold comparator is only provided as an output for external use such as large pulse event rejection or for accepting events that occur inside an energy window.

The output of the peakhold circuit is buffered and connected to the chip output through an analog multiplexer. Only one channel is connected to the output at a time. Each readout sequence consists of the peak and hold analog output, 4 bit chip address and 5 bit channel address. There is internal digital logic which allows automatic readout of the channels that have data (triggered), called the sparse readout mode [1].

B. RENA Chip Specifications

The RENA chip is a charge sensitive 32 channel mixed signal ASIC chip (Table I). The present version has a dynamic

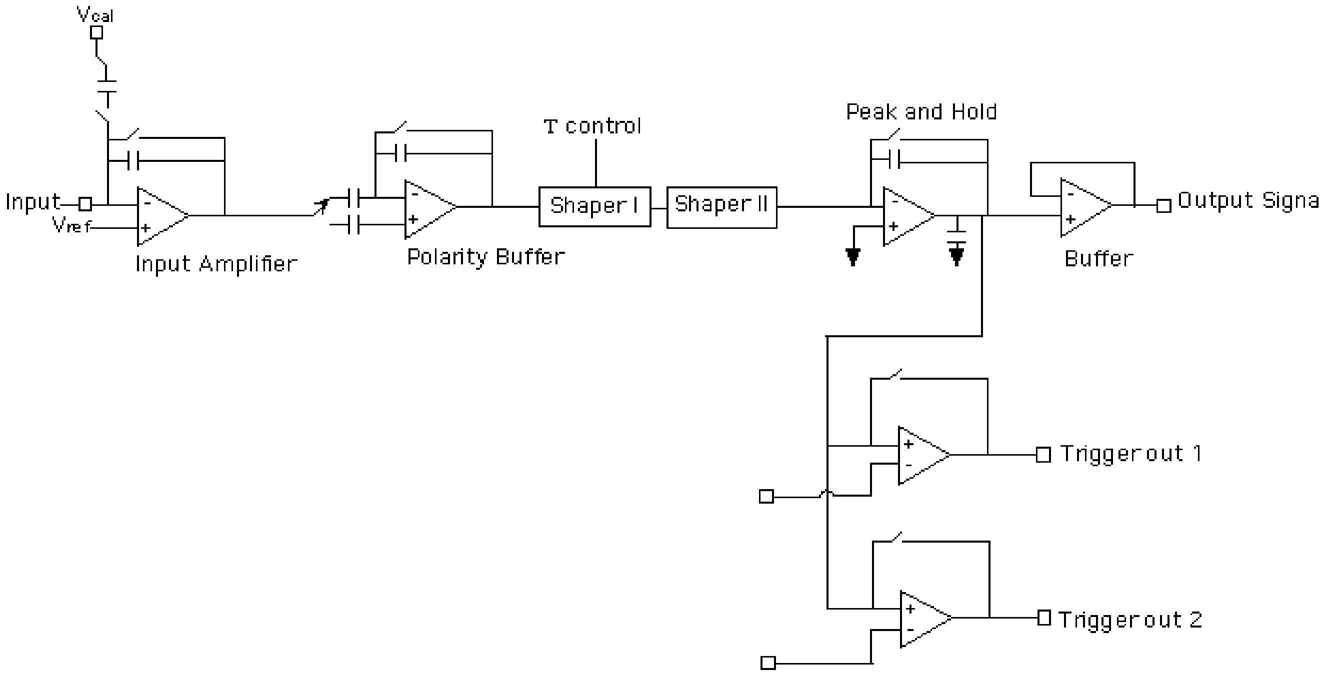

Figure 1. Block diagram of the analog section of the RENA chip.

range of 50,000 electrons and maximum output swing of 2 volts. The input is single ended with the input amplifier referenced to an external low noise reference voltage. Each of the 32 channels' peak and hold outputs are multiplexed to a single analog output buffer.

The RENA chip has several different readout modes. In the SPARSE mode only channels that are enabled and triggered (have a signal above the threshold of the low level comparator) are readout. In the GLOBAL mode all channels that are externally enabled are readout. The SELECT ALL mode allows an external trigger to initiate readout of all enabled channels. Normally once a channel is triggered the rest of the channels get disabled within 2 to 40 ns. In the EXTERNAL DELAY TRIGGER mode the disabling of the other channels, after a trigger, can be delayed by an external signal. In the NEIGHBOR mode the nearest (adjacent) channels immediately above and below the channel that has valid data is also readout. This mode is important if charge sharing between detector channels is expected to happen with significant probability.

Up to sixteen RENA chips can be daisy chained together. When 2 to 16 RENA chips are daisy chained they can be read out as if they are a single chip with 32 to 512 channels.

II. TESTS DONE USING CdZnTe PAD DETECTOR ARRAY

A. RENA Chip Mounting

Figure 2 shows the second version of the RENA chip mounted on a low noise ceramic carrier. A dime is used to show the size. The output pad pitch is fanned out to 0.5 mm to accommodate PCB mounting and easy connection to external detectors with ultrasonic wire bonding. The ceramic carrier was designed to abut with each other so that a long chain of detectors such as silicon strip detectors can be mounted to them. If the silicon strip or other detectors have a pitch less than 0.5 mm, then the chip can be directly mounted onto the PCB next to the detector strips or pads.

Table I. RENA chip preliminary specifications.

Number of channels	32
Trigger modes	Self trigger: A channel will be read when hit Global trigger: All channels read upon any hit Neighbor readout: Adjacent channels also External delay trigger: Delay channel disable Select all: Read enabled channels on external trigger
Trigger threshold	Voltage input, 1.5 V to 3.5 V
Readout data	Channel address, pulse height and overload bit
Readout time	475 ns (1% settling time) per channel
Daisy chain	up to 16 chips can be daisy chained
Power	About 175 mW per chip
Test output modes	Enable any one channel Select peakhold or follow shaped output
Peaking time	0.4, 0.73, 1.06, 1.34, 1.73, 3.17, 4.61 or 6.05 µs
Dynamic range	1.25 ke to 50 ke input for 1.5 to 3.5 V output
Input referred noise	120 e rms @ 0 pF

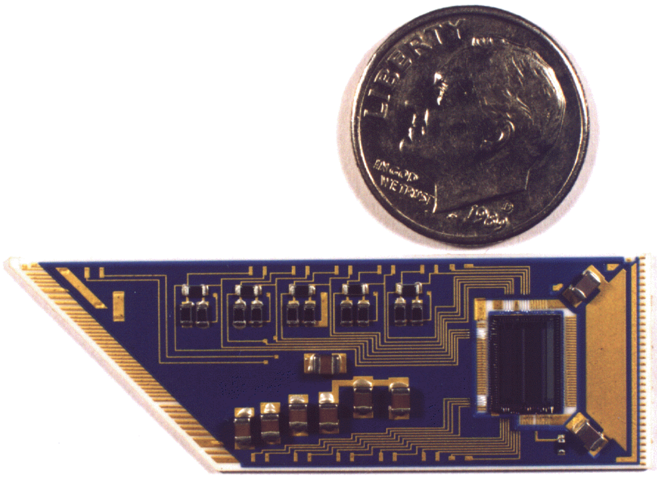

Figure 2. A RENA chip mounted on a ceramic carrier that is capable of accepting detector outputs with a pitch of ≥ 0.5 mm.

B. CdZnTe Two Dimensional Pad Array

Figure 3 shows the CdZnTe two-dimensional pad array used in testing the RENA chip. There are 32 pads (4 x 8) with a 3 mm pitch. One RENA chip can read all the 32 pads at the same time. The pads are not seen in this photograph as they are underneath facing the ceramic detector carrier.

Figure 3. A position sensitive CdZnTe pad detector with 32 (4 x 8) pads used for testing the prototype RENA chip.

C. RENA Chip Test Results

Preliminary tests of the RENA chip have been performed which included its functionality and noise characteristics.

The CdZnTe detector shown above was used in conjunction with the RENA chip to obtain preliminary x-ray spectra of ^{241}Am, one of which is shown in Figure 4. The 59.5 keV peak has a width of about 400 electrons RMS. This is the first spectra we have seen obtained from a CZT detector using a multi channel mixed signal ASIC chip with self trigger output.

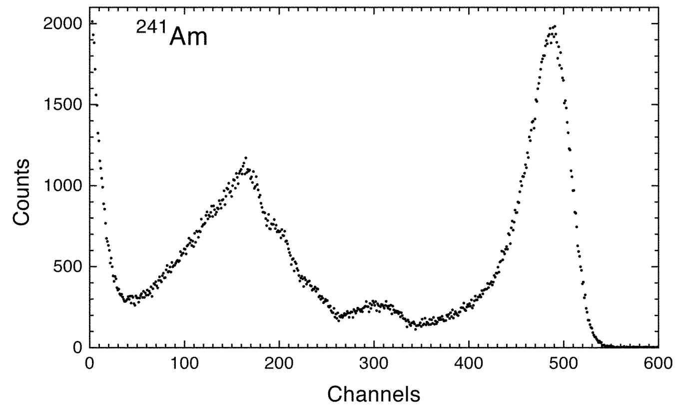

Figure 4. A preliminary spectrum of ^{241}Am obtained with the CdZnTe pad detector mounted on to a prototype RENA chip. The peakhold output is digitized using a 16 bit ADC where the upper 12 bits are used.

The output of the peakhold circuit was used in this study and it was digitized using a PC based 16 bit ADC. To overcome the linearization problem of non-nuclear ADC modules only the upper 12 bits were used.

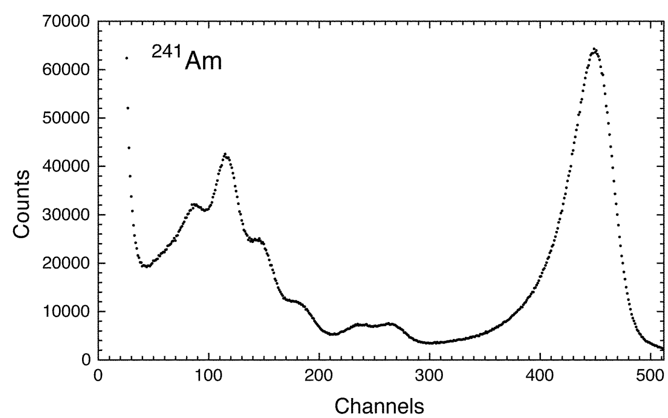

Figure 5. A preliminary spectrum of ^{241}Am obtained with the CdZnTe pad detector mounted on to a prototype RENA chip. The peakhold output is not used. The spectrum is obtained using the follower mode on RENA and the shaped output is analyzed using an external pulse height analyzer.

To check how good the analog section of the RENA chip another test was made by putting the chip into the follower mode where the peakhold is disabled and the shaped output signal of the selected channel appears at the output of the chip. This output is then amplified and put into a Tennelec pulse height analyzer. The resultant spectrum is given in Figure 5.

The spectrum in Figure 5 is less noisy than the spectrum in Figure 4. This shows that the analog section of the RENA chip has excellent noise characteristics. The difference between the two spectra could be due to external electronic circuitry and/or printed circuit board (PCB) layout. Also the peak detector circuit response may be affected by input signals with shaped pulse heights very near the lowest threshold comparator settings. This effect is not important for input signals above about 20 keV for CdZnTe detectors. Work is in progress to understand and correct this effect on the test PCB or in the next RENA version scheduled for fabrication in the first quarter of 1998.

Measurements on the gain linearity over the entire operating range of the RENA chip have been performed. The measurements were performed by supplying a pulse to the test input of the chip and measuring the voltage output. The results are shown in Figure 6 and indicate that the linearity of the gain is very good. Also of importance is the slope of the linearity curve which yields the gain of the RENA chip. From the chip design the gain for a test pulse is estimated to be 12. The slope of the curve is 0.0124 (volts /millivolt) which gives a gain of 12.4, in good agreement with the predicted value.

III. CONCLUSION

A general purpose front end electronics for solid state detectors and other charge output devices has been developed. The present chip is optimized for 6 pF input capacitance. Other versions are expected to be optimized for lower or higher input capacitance. In the future we plan to include an on board high accuracy ADC for full digital output. Custom modification and optimization for specific applications is also straight forward. Radiation hard versions can be fabricated for application in high radiation environments.

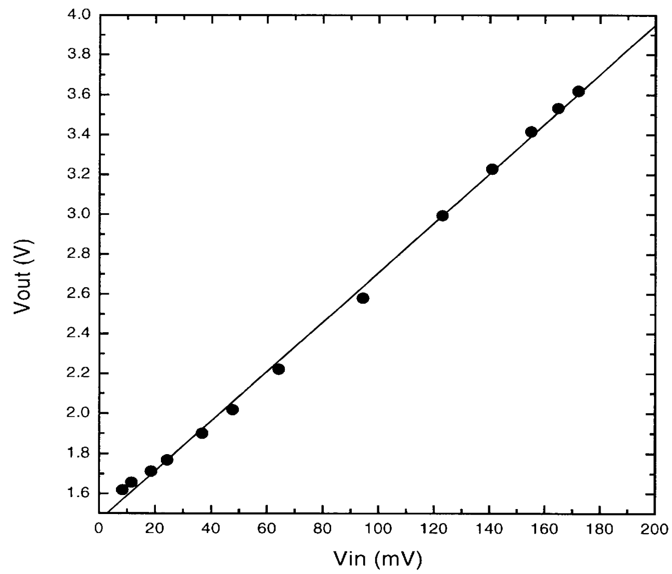

Figure 6. Output voltage vs. input test pulse voltage gain curve.

IV. ACKNOWLEDGMENTS

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V. REFERENCES

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